

In re Patent Application of:
VINSON ET AL.
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In the Specification:

Please replace paragraph [0026] on page 11 with the following rewritten paragraph:

[0026] FIG. 4 illustrates a fragmentary, partial sectional view of a decoupling capacitor subassembly 30 that is mounted directly onto an integrated ~~circuit~~ 31 circuit or similar semiconductor die 14 that is shown as a bare die positioned on a multilayer ceramic substrate 12 formed from green tape layers (shown by dashed lines) or other techniques as known to those skilled in the art. Substrate bonding pads 20 are positioned on the substrate as known to those skilled in the art. The integrated circuit or other semiconductor die 14, as illustrated, is formed from silicon, as known to those skilled in the art. As shown, the decoupling capacitor subassembly is formed such that the decoupling capacitor 16 is mounted on a capacitor carrier 34 that is formed as an aluminum nitride substrate layer that is preferably about 10 mil thick, as a non-limiting example, and can range from as little as 5 mil to about 50 mil thickness, as an example. The ceramic decoupling capacitor, capacitor carrier and integrated circuit chip are all substantially matched as to their coefficient of thermal expansion (CTE). The ceramic substrate is also preferably CTE matched.